Laboratory 2

(Due date: **011**: October 1st, **005**: October 2nd, **007**: October 3rd)

Objectives

- ✓ Use the Structural Description on VHDL.
- ✓ Test arithmetic circuits on an FPGA.

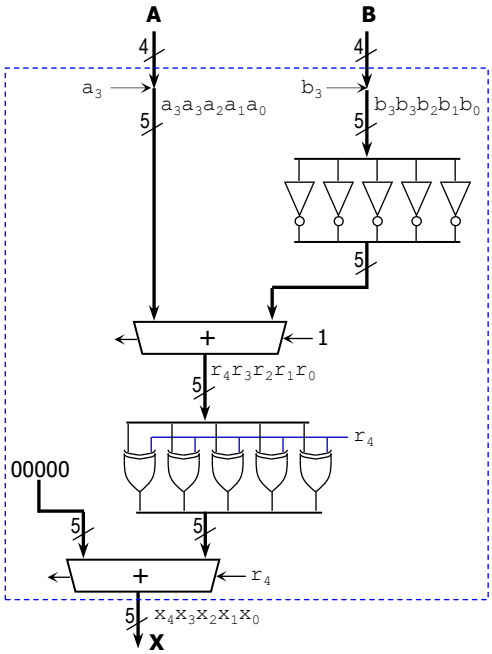
VHDL Coding

- ✓ Refer to the Tutorial: VHDL for FPGAs for a list of examples.

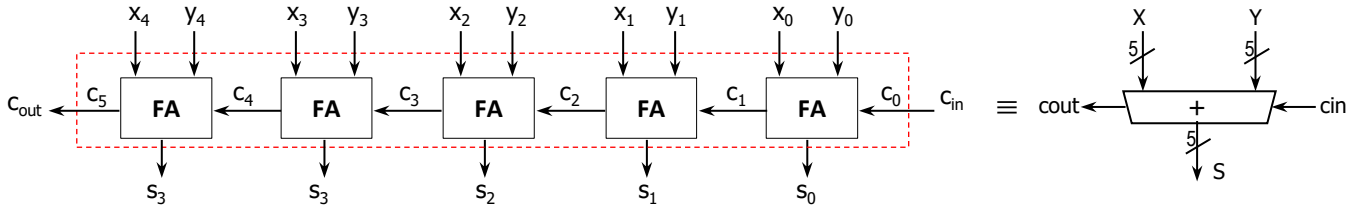
First Activity: Design and Simulation (70/100)

Design Problem

- **Absolute value of the difference**. The operands (A and B) are 4-bit signed (2C) numbers. The operation is $X = |A - B|$.
- This circuit can be built out of two 5-bit adders, 5 NOT gates, and 5 XOR gates as depicted in the figure.
  - ✓ The output of the top 5-bit adder is $R = A - B$, where $R = r_4 r_3 r_2 r_1 r_0$.
    - For this adder: cin=1, cout is unused.
  - ✓ The output of the bottom 5-bit adder is $X = |R| = |A - B|$.
    - For this adder: cin=r_4, cout is unused.
  - ✓ Given the result $X = x_4 x_3 x_2 x_1 x_0$, it can be demonstrated that $x_4 = 0$.

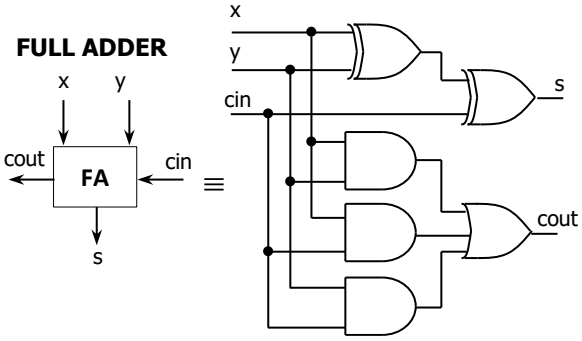


- The figure below depicts the internal architecture of the 4-bit adder and the 5-bit adder. The full adder (FA) circuit is also shown.

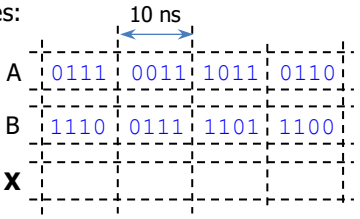


Procedure

- **Vivado: Complete the following steps**:
  - ✓ Create a new Vivado Project. Select the corresponding Artix-7 FPGA device (e.g.: the XC7A50T-1CSG324 FPGA device for the Nexys A7-50T).
  - ✓ Write the VHDL code for this circuit.
    - Use the Structural Description: Create a separate `.vhd` file for the Full Adder, the 5-bit adder, and the top file (absolute value of the difference of two 4-bit signed numbers).



  - ✓ Write the VHDL testbench to test the circuit for the following cases:
    - **A**=0x7, **B**=0xE → **X**=01001
    - **A**=0x3, **B**=0x7 → **X**=00100
    - **A**=0xB, **B**=0xD → **X**=00010
    - **A**=0x6, **B**=0xC → **X**=01010



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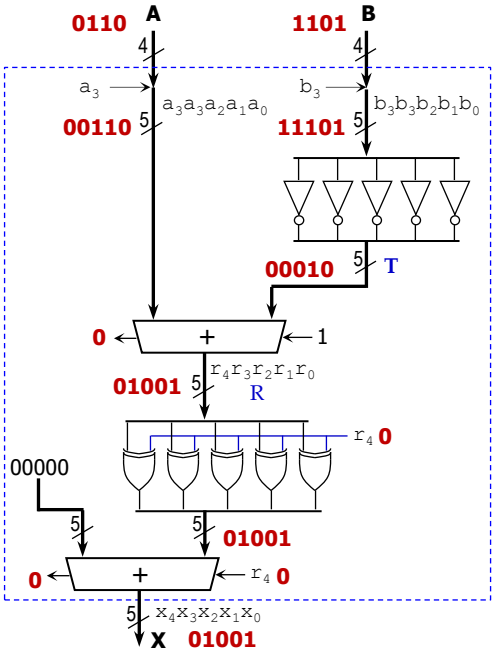
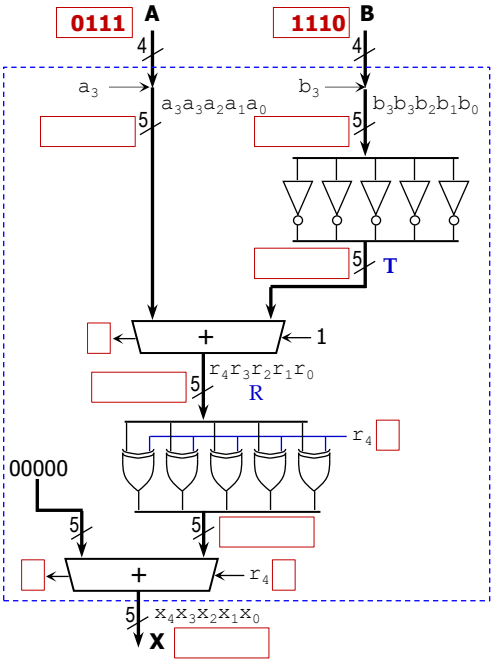
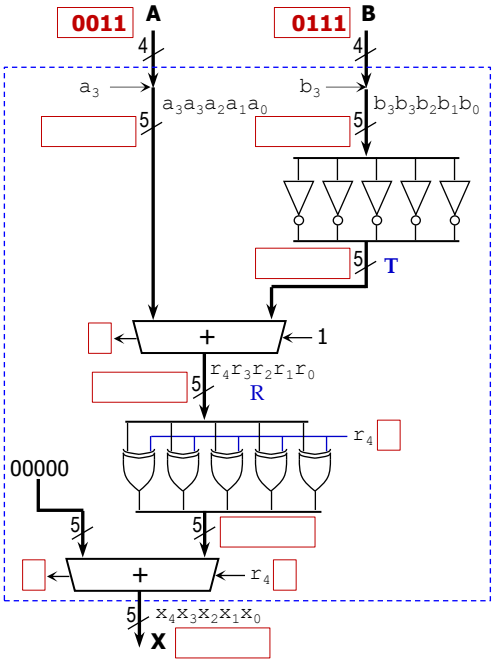
TA: Alex Fillmore, Joseph Volvic, Madhusudhan Swargam

- ✓ Perform Functional Simulation of your design. **Demonstrate this to your TA**.
  - Add the internal signals (e.g.: R) to the waveform view. Go to: SCOPE window: testbench → UUT. Then go to Objects Window → Signal(s) → Add to Wave Window. Finally, re-run the simulation.
    - This step is extremely useful when debugging your circuit. Your circuit might be cleared of syntax errors, but there might still be errors that can be difficult to spot. By tracing the internal signals, we can determine where the error is located in the circuit.
    - In this circuit, for a given set of input values, we can manually compute the expected output values and internal signal values. For example, the figure shows the output and internal signal values when A=0110 and B=1101. We can then compare those output/internal values with those provided by the simulation:
      - If the output X is incorrect (simulation results don't match the expected values), then look at the value of the signal R.
        - If the value of R is correct (i.e., simulation results match the calculated values), then the error is located in the lower 5-bit adder and/or the XOR gates.
        - If the value of R is incorrect, then the error is on the upper 5-bit adder and/or the NOT gates.



  - **For the following two sets of inputs**:
    - Complete the expected values (red boxes) of the listed internal signals (and the output signal).
    - Then, run the simulation and compare the values in the simulation waveform with the ones you computed. This will help you figure out where the errors (if any) are located at.





- ✓ **Demonstrate this to your TA**. _____ (TA signature)

SECOND ACTIVITY: TESTING (30/100)

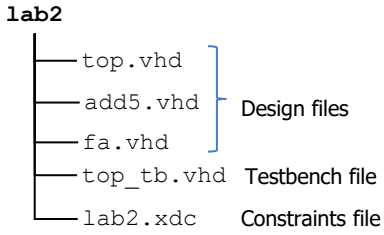
- **Vivado: complete the following steps:**
  - ✓ I/O Assignment: Generate the XDC file associated with your board.
    - Suggestion:

Board pin names	SW7–SW4	SW3–SW0	LED5	LED4	LED3	LED2	LED1	LED0
Signal names in code	A_3–A_0	B_3–B_0	X_5	X_4	X_3	X_2	X_1	X_0

    - The board pin names are used by all the listed boards (Nexys A7-50T/A7-100T, Basys 3, Nexys 4/DDR). The I/Os listed here are all active high.
  - ✓ Implement your design (Run Implementation) and run Timing Simulation.
  - ✓ Generate and download the bitstream on the FPGA, then perform testing (the 4 cases in your VHDL testbench). **Demonstrate this to your TA**.

SUBMISSION

- Submit to Moodle (an assignment will be created):
  - ✓ This lab sheet (as a .pdf) completed and signed off by the TA (or instructor).
  - ✓ (As a .zip file) The five generated files: VHDL code (3 files), VHDL testbench, and XDC file. DO NOT submit the whole Vivado Project.
    - Your .zip file should only include one folder. Do not include subdirectories.
    - It is strongly recommended that all your design files, testbench, and constraints file be located in a single directory. This will allow for a smooth experience with Vivado.
    - You should only submit your source files AFTER you have demoed your work. Submission of work files without demoing will be assigned NO CREDIT.



TA signature: _____ **Date:** _____